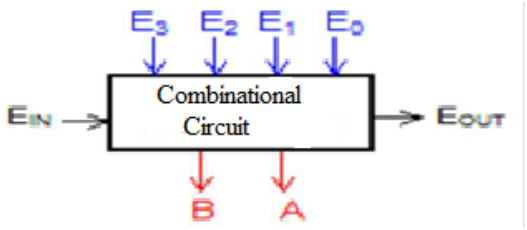
Assignment N° 3

Encoders, Decoders, Converters, Multiplexers, Demultiplexers

Exercise 01:

Consider a combinational circuit with 5 input lines and 3 output lines, as shown in the figure below



It functions as follows:

- When only one input line among E_0, E_1, E_2, E_3 is at high level (=1), its number (0, 1, 2 or 3) is coded in binary on the outputs BA.
- If several lines are simultaneously high (=1), the circuit codes the highest input number.
- If all the input lines are at low level (=0), the circuit codes BA=00, but it is signaled by E_{OUT}=1 that means this code is not valid. In all other cases E_{OUT}=0.
- The operations described so far is observed when E_{IN}=1. If E_{IN}=0, we have: B=A=E_{OUT}=0.

1- Give the truth table of this combinational circuit (priority encoder).

2- Give the logical expressions of the outputs A, B and E_{OUT} according to the inputs E_0, E_1, E_2, E_3 and E_{IN}.

3- Deduce the logic circuit of this encoder.

4- How can get an 8-input priority encoder from two priority encoders and some necessary logic gates.

Exercise 02: Parity of a number

We want to design a circuit that detects the parity of a binary number represented in 3 bits $(ABC)_2$. The output P will be 0 if the number of $(ABC)_2$ in input is even and 1 otherwise.

1. Write the corresponding truth table.
2. Use an 8x1 multiplexer to realize this function.

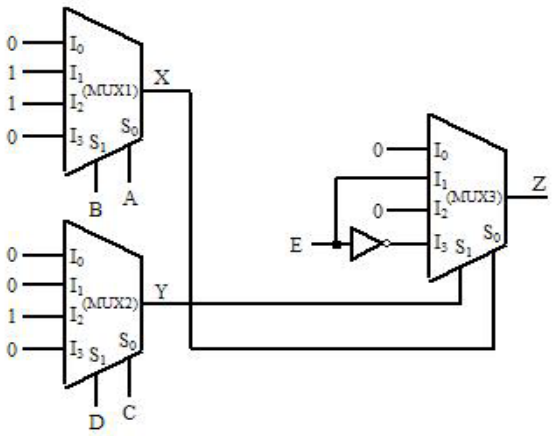
Exercise 03:

Consider the assembly in the figure. It is made from three multiplexers MUX-1, MUX-2 and MUX-3 each with 4 inputs.

1- Give the general scheme of MUX 4 to 1 and its truth table.

2- Give the logical expression of Z as a function of A, B, C, D and E.

3-Write this expression only with exclusive OR (XOR).



Exercise 04:

A. Perform the following Boolean functions using a decoder (3 to 8) and logic gates:

$$F1 = \bar{A}B\bar{C} \qquad F2 = A\bar{B}\bar{C} \qquad F3 = AB\bar{C} + \bar{B}\bar{C}D$$

B. Using an 8 to 1 multiplexer and logic gates, perform the following logic function

$$F4 = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}CD + ABCD$$

C. Perform the following Boolean function using a decoder (3 to 8) and logic gates:

$$F5 = AB + A\bar{B}C + ABC$$

D. Using a 4 to 1 multiplexer and logic gates, perform the following logic function

$$F6 = \bar{A}\bar{B}\bar{C}D + \bar{A}BC + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}D + ABC + AB\bar{C}$$

E. Using a 1 to 8 demultiplexer and logic gates, perform the following logic function

$$F4 = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}CD + ABCD$$

F. Implement a multiplexer (MUX 4 to 1) using two multiplexer (MUX 2 to 1)

Exercise 05:

1- The Figure-1 shows a comparator of two 1-bit binary numbers x_i and y_i.

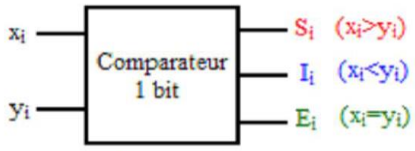


Figure-1

- Give the logical expressions of the outputs S_i, I_i, E_i?

2- We want to design a comparator of two three-bit binary numbers $X=x_2x_1x_0$ and $Y=y_2y_1y_0$, whose block diagram is given in the figure-2. Note that x_0 and y_0 are the least significant bits.

- Give the logical expressions of the outputs S, I and E according to the outputs S_i, I_i, E_i of the 1-bit comparator, with i=0, 1, 2.

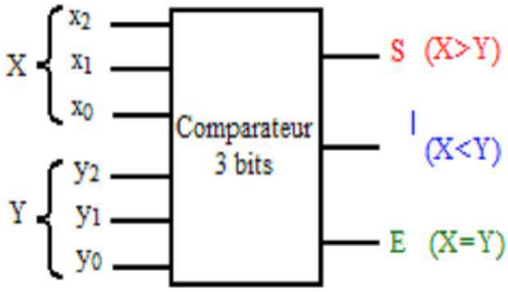


Figure-2

3- We want to display the outputs (S, I, E) of the comparator on a 7-segment display with common cathodes using a converter, as shown in the figure-3a, and this to obtain the display given by the figure-3b.

- Give the transcoding table and logical expressions allowing the passage from the S, I, E code to the 7-segment code.

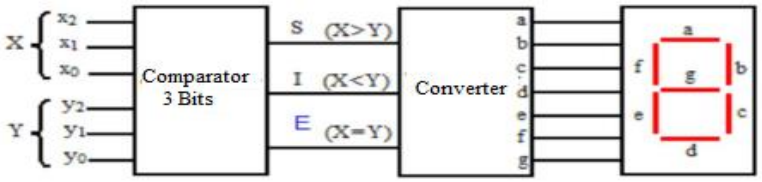


Figure-3a

Figure-3b

Exercise 06 : Consider a decoder with 2 selection (address) inputs (a_1a_0) and a validation input E.

1- Give: the truth table and the detailed equations of its outputs S_0, S1, S2, and S_3.
2- Give the detailed diagram of this decoder.
3- Design a 4 to 16 decoder using 3 to 8 decoders?

Exercise 07 :

- Design a circuit that converts BCD code to 3-excess binary code.
- Give the truth table and the logic circuit of a converter of 3-bit natural binary code to Gray code.
- Using 4-bits comparators 7485 design a 32-bits comparator